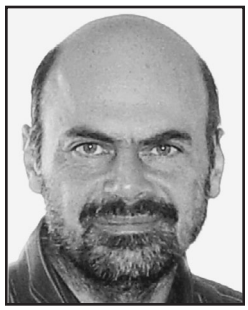
Session 31 Overview

Very High-Speed ADCs and DACs



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High-speed ADCs and DACs are gaining increasing importance due to the ever increasing bandwidth reqirements of modern communication services. Typical examples of such high-speed applications are serial links, UWB devices, and storage systems. Most of these systems do not require very high resolution, but high speed is of crucial importance. At the same time the power has to be kept low in order to enable single-chip and even portable solutions.

The nine presentations in this session are grouped into six ADC and three DAC papers. ADC resolutions are in the range of 4 to 6 bits with the exception of the last one which is an 11-bit converter. All DACs run at RF frequencies except for the last one, which demonstrates a novel linearization technique for high-resolution DACs.

Paper 31.1 is targeted at high-speed (1.25GS/s) and low-resolution (4 bits) applications and has a superior power efficiency. To achieve this goal the flash-based design uses an unusual comparator architecture that incorporates offset correction and is capable of avoiding the reference ladder.

In contrast to that, the ADC in Paper 31.3 goes up to 4GS/s. It is also based on the flash architecture but incorporates inductors in the comparators to gain an extra kick in speed.

Papers 31.2 and 31.5 describe 6-bit converters which are typically needed for UWB and storage systems. Paper 31.2 incorporates a subranging technology. In order to achieve low power dissipation it uses an offset-calibration technique that accounts for all the errors in the complete signal chain. Additionally, it uses a range-switching scheme that is more insensitive to metastability than the usual approach. The ADC described in Paper 31.5 demonstrates superior power efficiency in using a time-interleaved non-binary SAR architecture. Asynchronous design techniques enable optimized speed performance.

The converter presented in Paper 31.4 runs at 22GS/s, therefore, enabling digital equalization of 10Gb/s serial links. The chip is fabricated in a 0.13µm SiGe BiCMOS technology and has a sufficiently low power that enables the integration of a complete 4-channel solution on one die. It also uses an active offset control.

The ADC papers are concluded by Paper 31.6 that presents a 1GS/s 11-bit ADC running at only 250mW. This is achieved by time interleaving of 4 double-sampled pipelined channels. The paper specifically addresses the problem of sampling-time mismatch in using a distributed double switch.

The last three papers are about DACs. The chip presented in Paper 31.7 incorporates frequency generation, filtering, and up-conversion in a compact building block consisting of a current steering semi-digital filter implemented as an RF-DAC. In contrast to that, the circuit in Paper 31.8 uses a very high-speed DAC (20GS/s) to directly form the output wave of an UWB transmitter.

The last paper, Paper 31.9, concludes the session by discussing a dynamic element matching scheme for binary-weighted structures. The technique is demonstrated for a 14-bit highly linear DAC.

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31.1 A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process **1:30 PM**
G. Van der Plas, IMEC, Leuven, Belgium

A high-speed 4b flash ADC in 90nm digital CMOS is presented that uses a dynamic offset-compensation scheme in its comparators. It achieves a sampling rate of 1.25GS/s with 3.7 ENOB (23.8dB SNDR) from dc to Nyquist while consuming 2.5mW. It has an energy per conversion step of 0.16pJ.

31.2 A 90nm CMOS 1.2V 6b 1GS/s Two-Step Subranging ADC **2:00 PM**
P. Figueiredo, Chipidea Microelectrónica, Porto Salvo, Portugal

A 1.2V 6b 1GS/s ADC is fabricated in a 90nm CMOS process, occupies 0.13mm^2, and consumes 55mW. This ADC uses background offset-calibration to enable the use of minimum-size devices in pre-amplifiers and comparators. A solution that guarantees fast selection of the important reference voltages, and halves the number of switches in the resistor ladder, further improves high-frequency performance.

31.3 A 4GS/s 4b Flash ADC in 0.18µm CMOS **2:30 PM**
S. Park, University of Michigan at Ann Arbor, Ann Arbor, MI

A 0.18µm CMOS 4GS/s non-interleaved 4b flash ADC is presented. A comparator with a 32×32µm^2 on-chip inductor extends sampling rate without extra power consumption. DAC trimming and comparator redundancy reduce DNL and INL to less than 0.15LSB and 0.24LSB, respectively. The measured ENOB is 3.84b and 3.48b at 3GS/s and 4GS/s, respectively. The ADC achieves a BER of less than 10^{-8}.

31.4 A 22GS/s 5b ADC in 130nm SiGe BiCMOS **2:45 PM**
P. Schvan, Nortel, Ottawa, Canada

A 22GS/s 5b ADC implemented in 130nm SiGe BiCMOS technology is presented. The ADC has 0.64V input range and achieves 4.4b and 3.5b ENOB with 34dB and 29dB SFDR at 5GHz and 7GHz input frequencies, respectively. Measured DNL and INL are <0.5LSB and BER is 10^{-4} at 22GS/s. The ADC consumes 3W from a 3.3V supply.

31.5 A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13µm CMOS **3:15 PM**
S-W. Chen, University of California, Berkeley, CA

A 1.2V 6b ADC using asynchronous processing with dual time interleaving and non-binary successive approximation achieves 600MS/s while dissipating 5.3mW in a 0.13µm CMOS process. A capacitive ladder network is used to reduce the input capacitance without compromising matching accuracy. The ADC occupies an active area of 0.12mm^2 and has an input 3dB BW of over 4GHz.

31.6 A 1GS/s 11b Time-Interleaved ADC in 0.13µm CMOS **3:45 PM**
S. Gupta, Teranetics, Santa Clara, CA

A time-interleaved ADC architecture that eliminates the need to correct timing offsets and is scalable to high sampling rates is presented. This 1GS/s 11b ADC has 55dB peak SNDR, consumes 250mW power, and occupies 3.5mm^2 area.

31.7 A Bandpass ΔΣ RF-DAC with Embedded FIR Reconstruction Filter **4:15 PM**
S. Taleie, Arizona State University, Tempe, AZ

A 1b bandpass ΔΣ DAC followed by a current steering FIR reconstruction filter and an embedded up-conversion mixer is presented. The RF DAC is implemented in 0.25µm digital CMOS, can be used in low-power digital-IF transmitters and eliminates the need for a transimpedance stage and a separate mixer. The RF DAC draws 49mA from a 2.5V supply, achieving -64.7dBc IM3 at 1.03GHz with an SFDR of 72dB in a 15MHz bandwidth.

31.8 A 0.36W 6b up to 20GS/s DAC for UWB Wave Formation **4:45 PM**
D. Baranauskas, Pulse~Link, Carlsbad, CA

A 6b up to 20GS/s DAC is presented. The DAC is used for direct synthesis of modulated waveforms for UWB communication. The DAC has a current-steering architecture for achieving 20GS/s, a 1.8V power supply, a 4:1 MUX for reducing the line data rate, and BIST. Fabricated in a SiGe process, it consumes 0.36W and has a FOM of 0.28pJ.

31.9 A 14b 100MS/s DAC with Fully Segmented Dyanmic Element Matching **5:00 PM**
K. Chan, University of California, San Diego, CA

A 14b 100MS/s Nyquist-rate DAC using a segmented dynamic-element-matching technique involving all the DAC elements is demonstrated. The DAC is implemented in a 0.18µm CMOS process and worst-case SFDRs across Nyquist bands are 74.4dB and 78.9dB for sample-rates of 100MS/s and 70Ms/s, respectively.